University of Arizona

Department of Electrical Engineering

Analog/hybrid Computer Laboratory

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1. ASTRAC II Project

The ASTRAC II iterative-differential-analyzer system was completed in the Fall of 1965 and is now operating on several research problems. The system comprises a fast patchbay-mounted 40-amplifier analog computer, digital timer/control unit, digital noise generator, and hard-wired digital four-parameter optimizer and statistics computer. Conversion equipment, including an 11-bit and a 4-bit bipolar analog-to-digital converter and four 8-bit digital-to-analog converter/multipliers are also completed, so that the machine is ready to connect to a general-purpose digital data processor, if such a machine should become available.

While many of ASTRAC II's novel analog and hybrid/analog-digital components have been described in our earlier publications, a complete system description and performance evaluation will be published in Fall, 1966, as H. R. Eckes' Ph.D. thesis. In addition, complete operator and maintenance manuals for the machine are being prepared.

2. Computer Applications

ASTRAC II is already being used by graduate students for term-paper projects in their courses on hybrid computation and random processes. Term-paper studies include

- Measurement of Linear System Impulse Response by Input-output Cross-correlation
- Amplitude-distribution Measurements
- Solution of Difference Equations
- Four-parameter Optimization Experiments

The purpose of these studies was, mainly, to explore the possibilities of the new computer and to test its accuracy. The results of these and other term-paper studies will be included in the ASTRAC II performance evaluation in Mr. Eckes' thesis.

Two Ph.D.-thesis projects, both well under way, constitute most of the ASTRAC II work load at this time.

(a) Predictive Optimization of Control Systems Using Pontryagin's Maximum Principle (Ph.D. thesis, R. Maybach).

A fast time-scale control-system model is iteratively optimized through solution of the two-point boundary-value problem involving state equations, adjoint equations and maximization of the Hamiltonian function. The ASTRAC II optimizer selects initial values to match the required far-end boundary conditions. Model initial conditions are updated by reference to the state variables of a control-system model simulated in real time, and the control variables for the real-time model are obtained from the optimized fast model. Mr. Maybach has already succeeded in optimizing a bang-bang control system at 500 iterations per second and is currently proceeding to higher-order systems, including a simple space-vehicle transfer-orbit problem.

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(b) Monte-Carlo Solution of Partial Differential Equations

(Ph.D. thesis, H. Handler)

The Monte-Carlo technique of solving elliptical and diffusion-type partial differential equations is made practical by the fast ASTRAC-II-type iterative differential analyzer. Mr. Handler has investigated the Monte-Carlo approach to several types of boundary conditions theoretically; has developed a simplified noise generator; and has solved the first simple boundary-value problem. Since ASTRAC II offers the possibility of making a thousand complete random walks per second, analog as well as digital averaging appears feasible, so that real-time plotting of solutions becomes possible. Analog averaging may also permit simulation of chemical or heat-transfer processes with analog input and output in real time.

Both Ph.D. studies are expected to be completed in the Fall of 1966.

3. Hybrid-computer Component and System Development: The LOCUST Project

As soon as ASTRAC II was even half finished, prospective users on the patchbay side of its bright blue front panel began to glare balefully at component and system designers working on the inner, or hardware, side of its cabinet. As in any good engineering organization, ideas for design improvements occur continuously; last Fall, for example, Bob Whigham was inspired to re-equalize ASTRAC II's 18 track-hold networks. He obtained a full octave increase in frequency response, but occasioned screams from the other side of the front panel.

With the start of the new semester, the writer (who admits to a slight hardware bias, but knows that system design requires application experience) cut the Gordian knot by freezing the ASTRAC II design and ordering even component-evaluation tests postponed until Summer, 1966. At the same time, all component and system development work was transferred to a separate small computer project to be called LOCUST (Low Cost Ultra-Speed Transistor). The LOCUST system will serve as a third-generation vehicle for post-ASTRAC component and system research; the LOCUST computer may be regarded as a small iterative differential analyzer in its own right, or as a patchbay-mounted subsystem to be added to existing slow analog-hybrid-computer installations, and should be of considerable interest as such.

The key features of the new project are a radical cost reduction effected through new packaging techniques and the use of integrated circuits. The cost reduction is of the order of three-to-one when compared to the ASTRAC system. The following development work is just starting:

(a) Development of Low-cost shielded Patchbays and Packaging System

1. A new scheme, employing home-made metal patchboards with very inexpensive diallyl phthallate patchbays (originally intended for digital computers) and using rows and columns of unused patchbay springs as grounded shield terminations, employs a $325 MacPanel 1600-point patch-bay receiver. This price should

be compared to the $1800-cost of the Electronic Associates, Inc., patchbay used in ASTRAC II and to the $3500-cost of comparable AMP, Inc., shielded patchbay systems available in the open market.

2. LOCUST digital circuits will consist entirely of monolithic integrated current-mode logic (Motorola MECL or similar RCA or Texas Instrument integrated circuits). The use of current-mode logic with 0.6-V logic levels should do away with the digital-noise problems encountered in ASTRAC II; at the same time, the use of integrated circuits permits the entire digital logic to be mounted on cards plugging directly into inexpensive digital patchbays without any interunit wiring whatsoever.

3. Development of a fast, feedforward operational amplifier, possibly employing monolithic integrated circuits in its intermediate and low-frequency sections. Some new circuit ideas are expected to reduce cost and improve performance; the use of FET input stages to replace chopper stabilization will also be investigated (M.S. thesis).

4. Development of an improved ASTRAC-II-type Mode-control switch. The new circuit will be controlled by the low-level integrated circuit logic and incorporates some new circuit ideas (M.S. thesis, Reames).

5. Replacement of coefficient-setting potentiometers with a digital-attenuator system fed from a central keyboard or by the associated digital computer (M.S. thesis, C. Pracht). Design of simplified digital attenuators switched by inexpensive reed relays and a system design for attenuator addressing and control is already under way.

The entire LOCUST project will be the subject of another Ph.D. thesis (B. Conant). The LOCUST patchbay system, design of the digital control circuits, and experimental quantities of amplifiers, mode-control switches, and digital attenuators will be completed in the Fall of 1966. Additional funds will be required to provide a sufficient number of amplifiers, switches, and attenuators for actual computation, but the LOCUST project is mainly intended to prove out hardware ideas.

4. Conference Participation and Publications

The writer was invited to be a panel member at the 1966 Spring Joint Computer Conference in Boston, Massachusetts; we were also invited in advance to present results of our ASTRAC II study on Partial Differential Equations at the 1966 Fall Joint Computer Conference in San Francisco. We also presented lectures on the ASTRAC II project to the Tucson IEEE section and to the staff of the Texas Medical Center in Houston.

At the 1965 Fall Joint Computer Conference R. Whigham's paper on the ASTRAC II quarter-square multiplier won a $50 prize and plaque presented by Simulation Councils, Inc. (an AFIPS society) for outstanding student papers. Mr. Whigham's paper was published in the August, 1965 issue of Simulation.

During the report period, 9/15/65 to 3/15/66, the following new reports were completed:

1. Maybach, R.: Generation of Inverse Functions by the Method of Steepest Descent (ACL Memo No. 100; submitted for publication). Not supported by NASA, but quoted here for reference.

2. Korn, G. A., and R. Whigham: Oscilloscope Display of Multiple Digital Signals (ACL Memo No. 116)

3. Korn, G. A.: Remarks at the 10th Anniversary of the International Analog-computer Association (ACL Memo No. 117)

4. ________________ : Improvised Multi-layer Packaging of Integrated-circuit Logic (ACL Memo No. 118)

The following project reports issued earlier were published:

5. Eckes, H. R.: A Fast Mode-control switch for Iterative Differential Analyzers, IEEETEC, February, 1966.

6. Whigham, R.: A Fast Analog Comparator for Hybrid Computation IEEETEC, October, 1965.

These publications will be combined into a fifth University of Arizona Engineering Experiment Station Report on the subject study, to be issued later in 1966. The writer's book Random-process Simulation and Measurements, which reviews much related material, was published by McGraw-Hill in February, 1966.

G A Korn, Prof. of EE
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